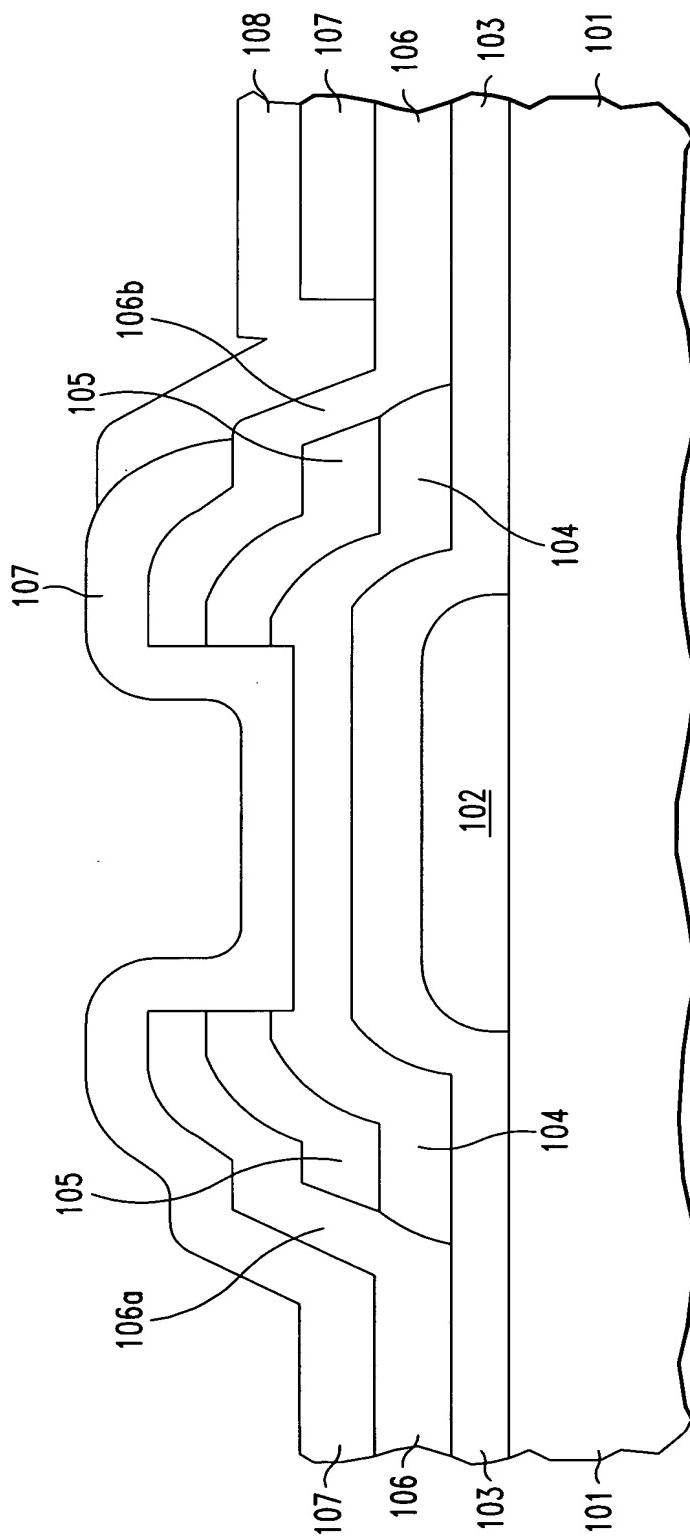


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**FIG. 1A (PRIOR ART)**

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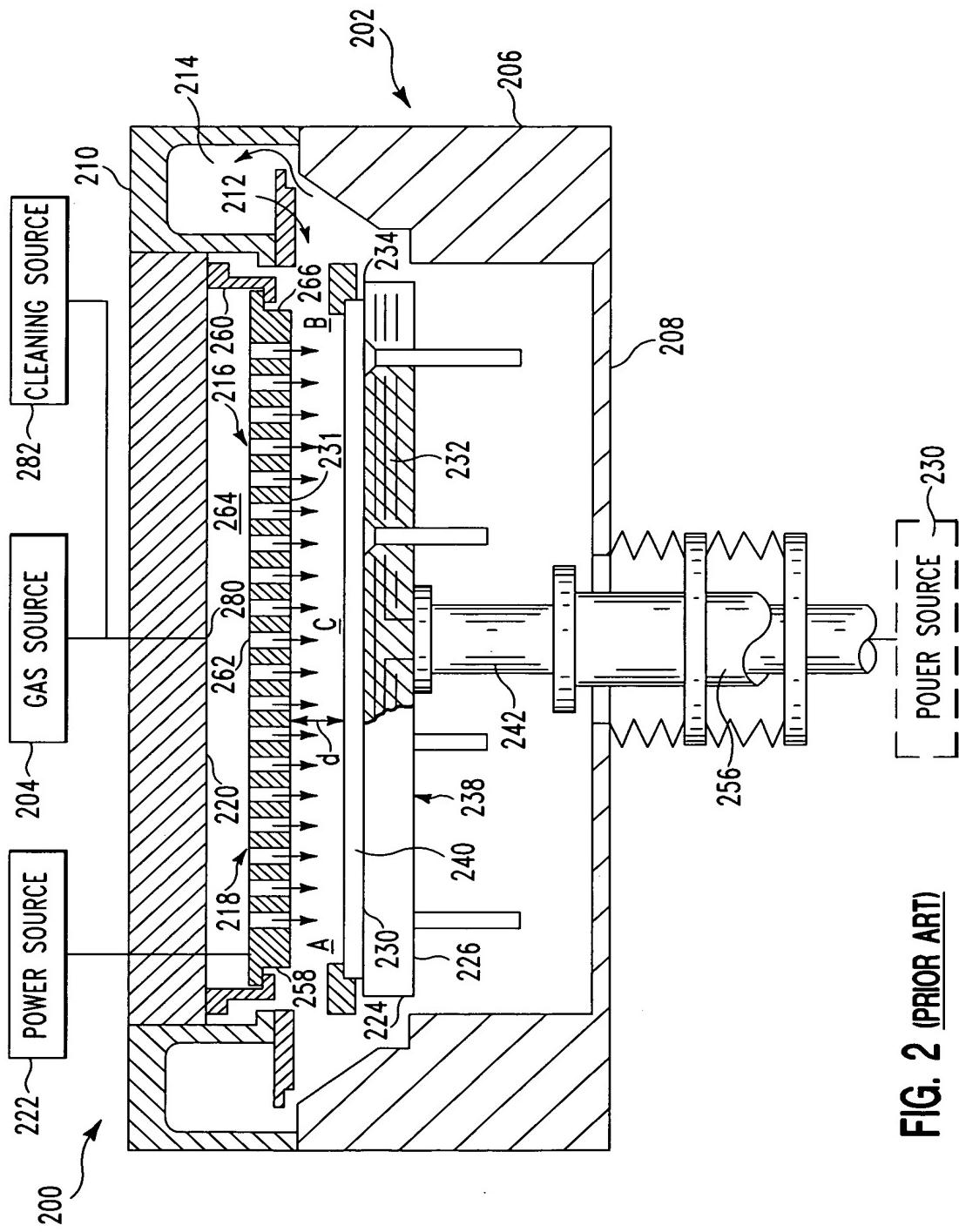
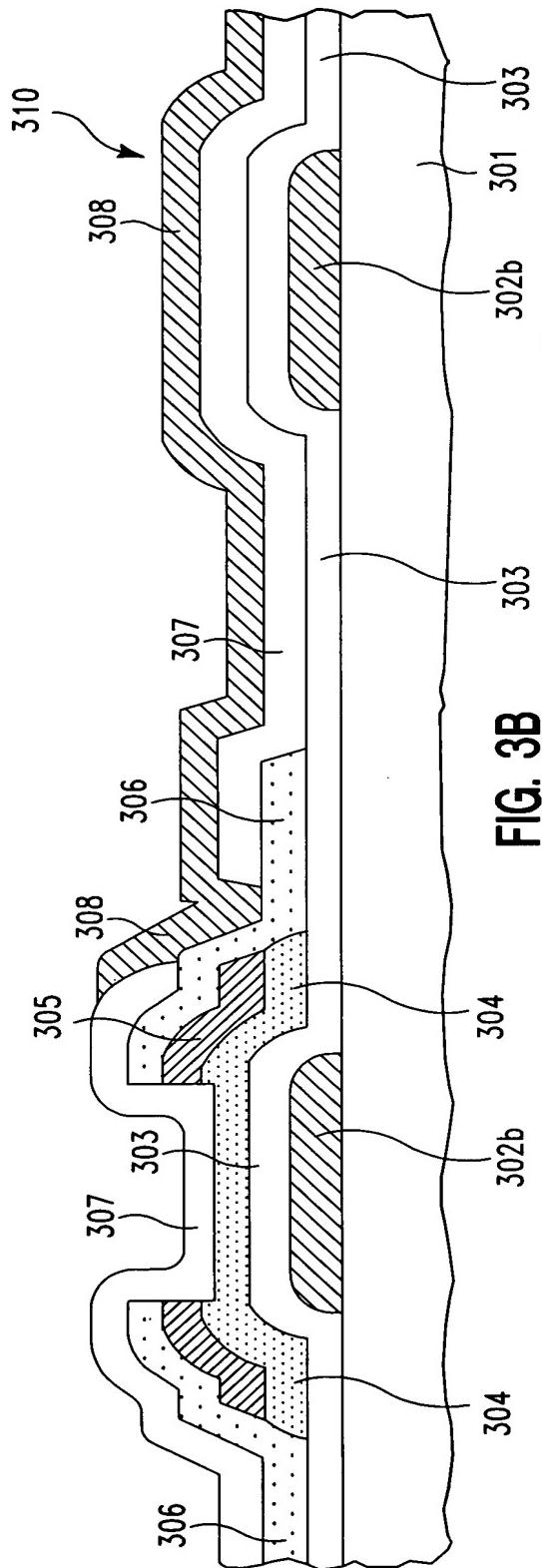


FIG. 2 (PRIOR ART)

300 {  
  | ITO Pattern(MASK5)  
  | ITO Sputtering  
  | Passivation Etch(MASK4)  
  | SiNx PECVD  
  | n+ a-Si Etch-Back  
  | S/D Pattern(MASK3)  
  | S/D Sputtering  
  |  $\alpha$ -Si Pattern(MASK2)  
  | n+a-Si/ $\alpha$ -Si/SiNx PECVD  
  | Gate Pattern(MASK1)  
  | Gate Metal Sputtering

**FIG. 3A**



**FIG. 3B**

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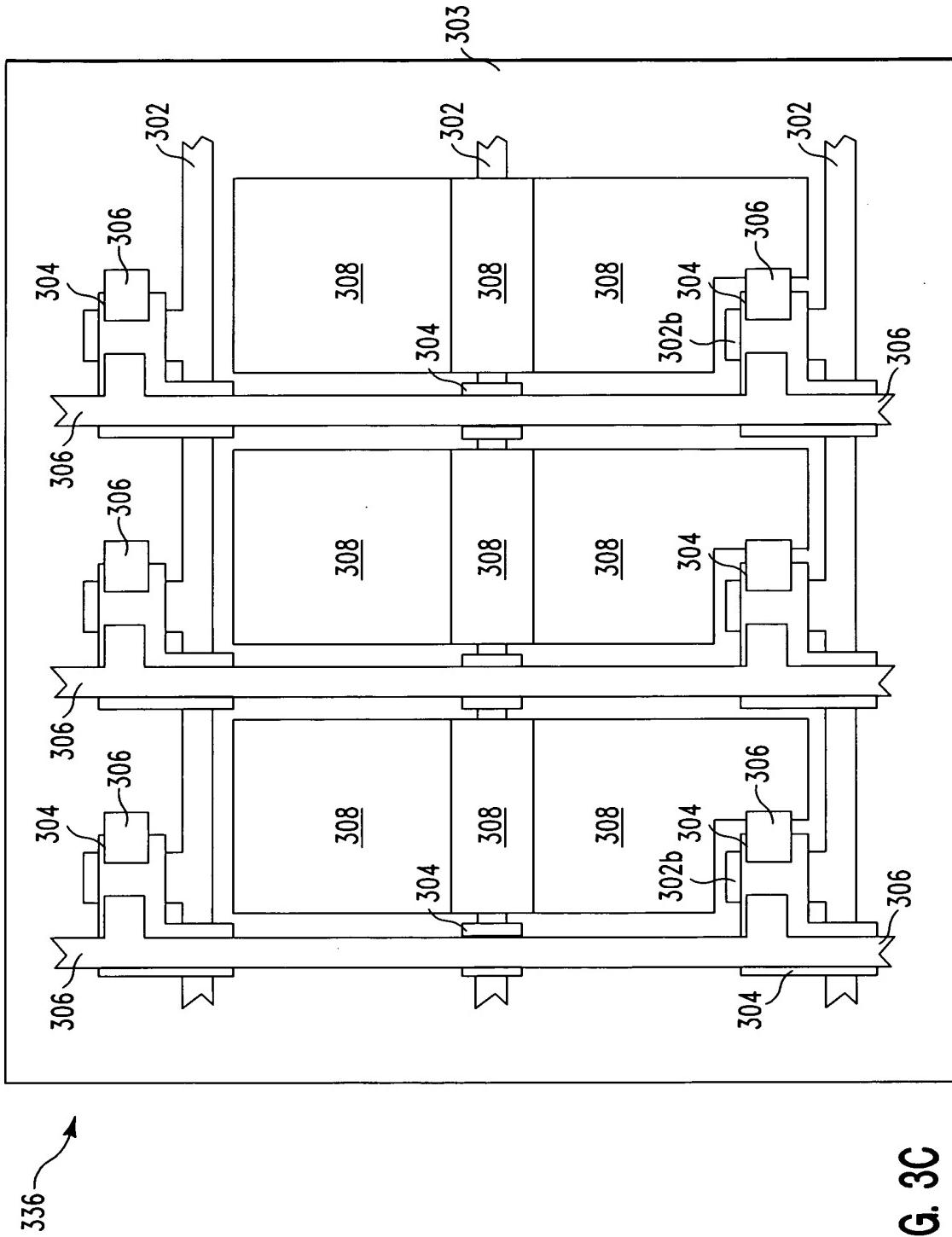
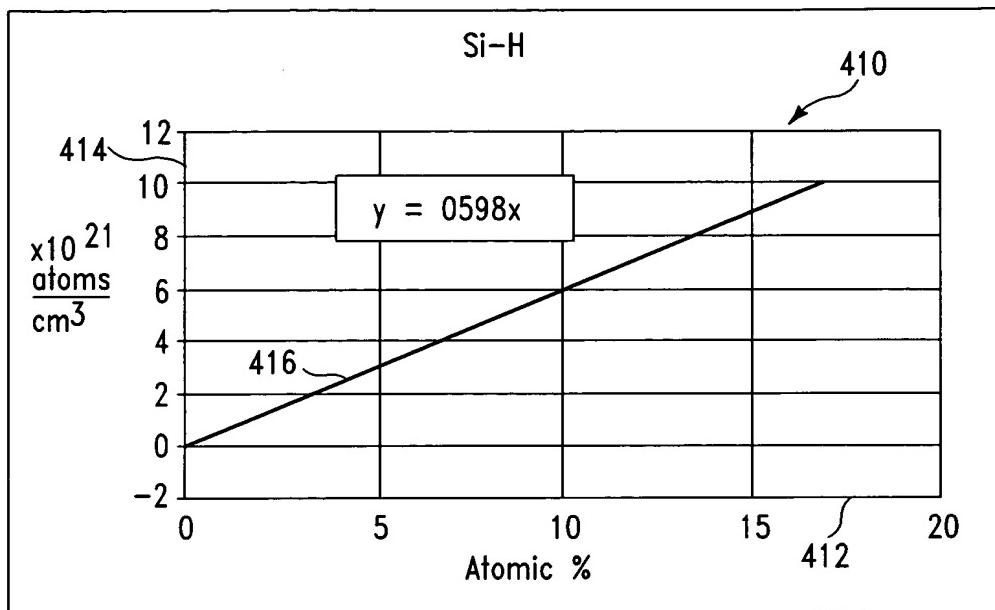


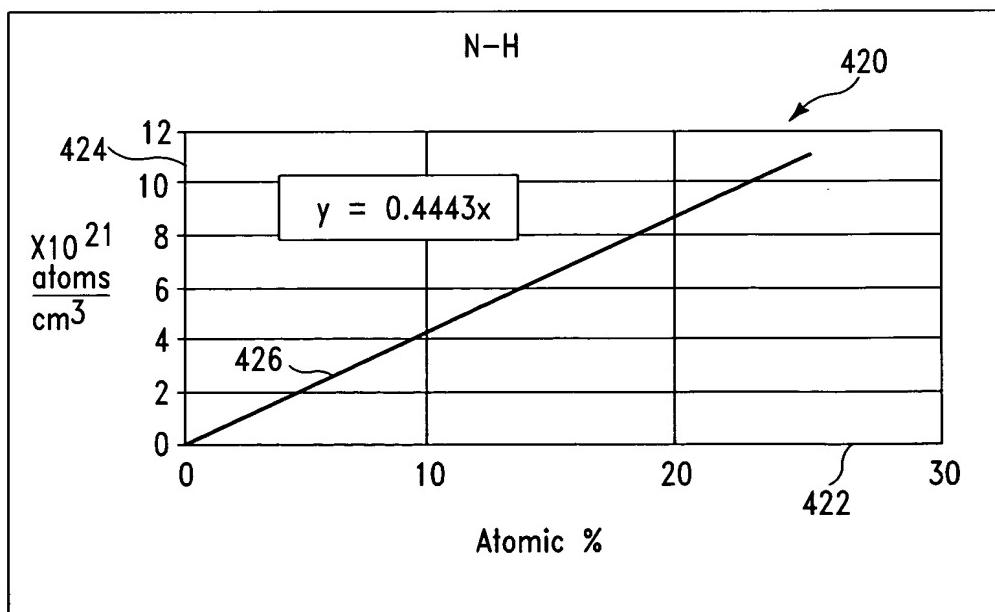
FIG. 3C

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**FIG. 4A**



**FIG. 4B**